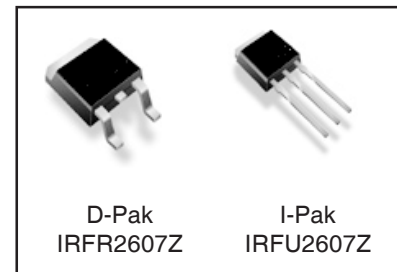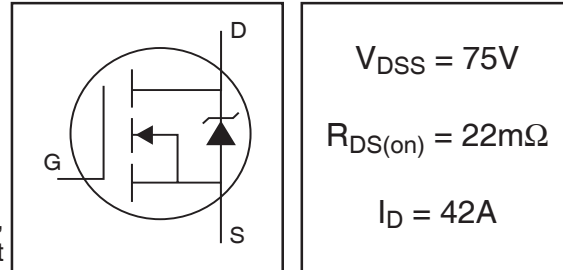**AUTOMOTIVE MOSFET**

IRFR2607Z
IRFU2607Z

Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating tempera-ture, fast switching speed and improved repetitive avalanche rating . These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

HEXFET® Power MOSFET

$V_{DSS} = 75V$

$R_{DS(on)} = 22m\Omega$

$I_D = 42A$

D-Pak
IRFR2607Z

I-Pak
IRFU2607Z

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	45	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	32	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	42	
I_{DM}	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.72	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy②	96	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy Tested Value ⑥	96	
I_{AR}	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	——	1.38	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) ⑦⑧	——	40	
$R_{\theta JA}$	Junction-to-Ambient ⑧	——	110	

9/21/04

IRFR/U2607Z

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.074	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	17.6	22	mΩ	V_{GS} = 10V, I_D = 30A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 50µA
gfs	Forward Transconductance	36	——	——	S	V_{DS} = 25V, I_D = 30A
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} = 75V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V
Q_g	Total Gate Charge	——	34	51		I_D = 30A
Q_{gs}	Gate-to-Source Charge	——	8.9	——	nC	V_{DS} = 60V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	14	——		V_{GS} = 10V ③
$t_{d(on)}$	Turn-On Delay Time	——	14	——		V_{DD} = 38V
t_r	Rise Time	——	59	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	39	——	ns	R_G = 15 Ω
t_f	Fall Time	——	28	——		V_{GS} = 10V ③
L_D	Internal Drain Inductance	——	4.5	——		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package
						and center of die contact
C_{iss}	Input Capacitance	——	1440	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	190	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	110	——	pF	f = 1.0MHz
C_{oss}	Output Capacitance	——	720	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	130	——		V_{GS} = 0V, V_{DS} = 60V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	230	——		V_{GS} = 0V, V_{DS} = 0V to 60V ④

Source-Drain Ratings and Characteristics

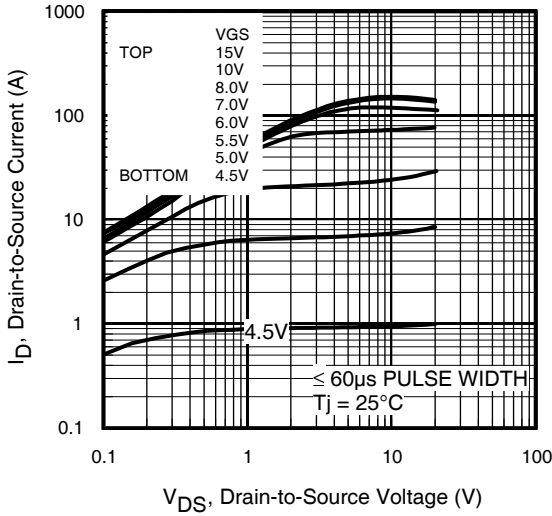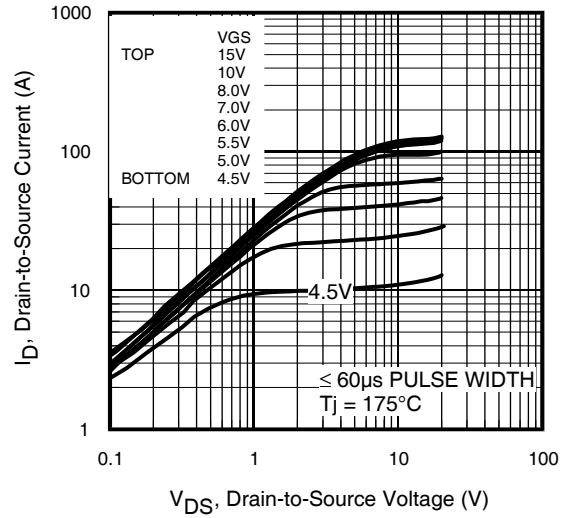|	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	45	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	180		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 30A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	30	45	ns	T_J = 25°C, I_F = 30A, V_{DD} = 38V
Q_{rr}	Reverse Recovery Charge	——	28	42	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Fig 1. Typical Output Characteristics
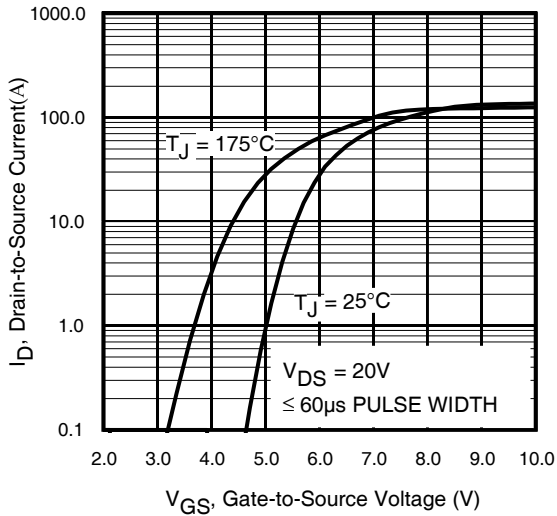

Fig 2. Typical Output Characteristics
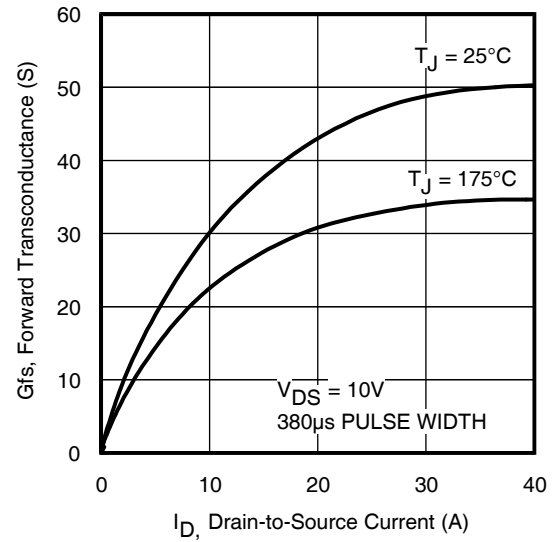

Fig 3. Typical Transfer Characteristics

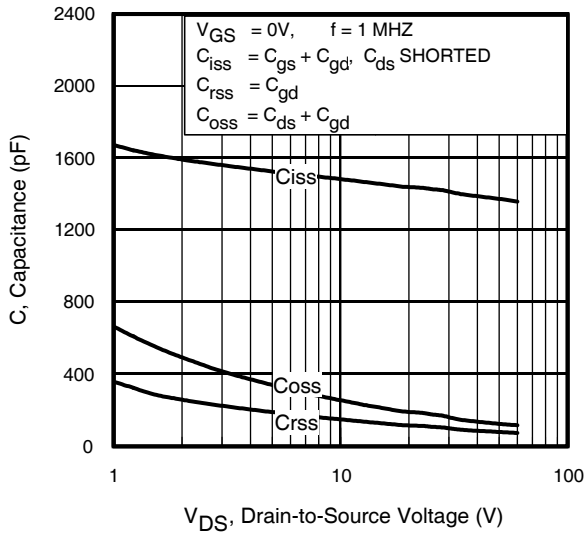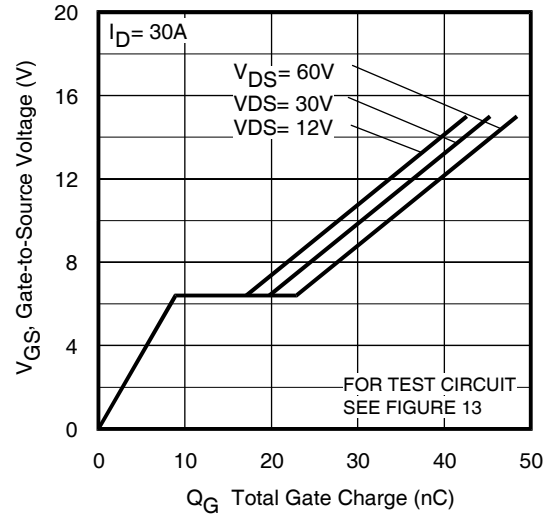**Fig 4.** Typical Forward Transconductance
Vs. Drain Current

IRFR/U2607Z

V_GS = 0V, f = 1 MHZ
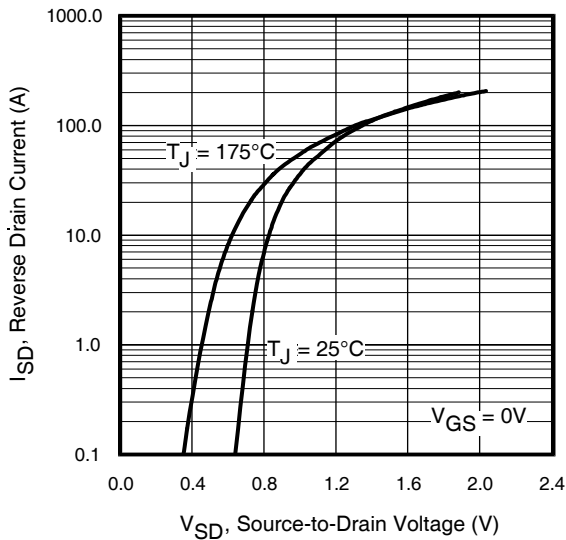C_iss = C_gs + C_gd, C_ds SHORTED
C_rss = C_gd
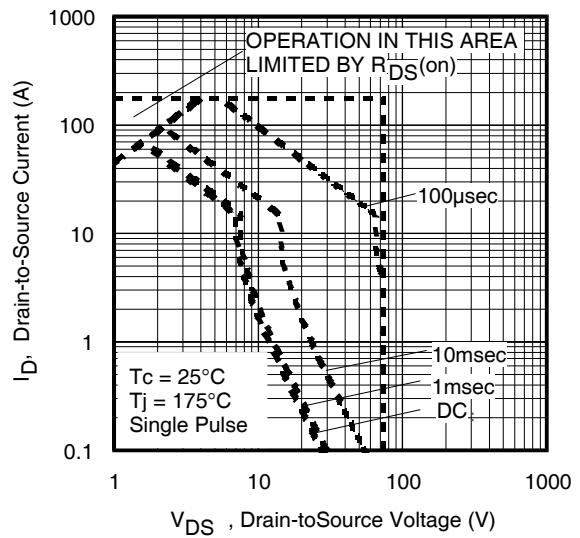C_oss = C_ds + C_gd

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

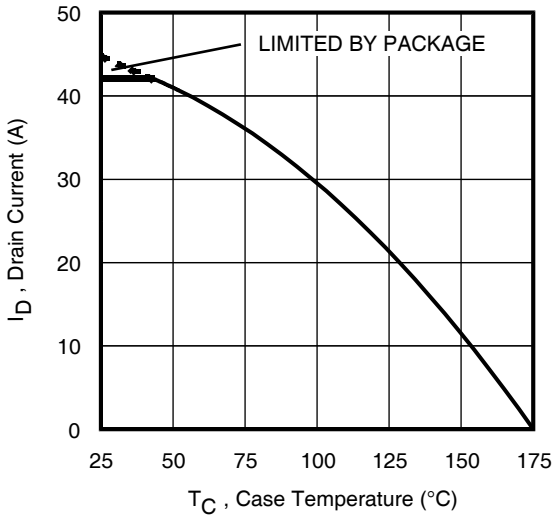**Fig 7.** Typical Source-Drain Diode Forward Voltage
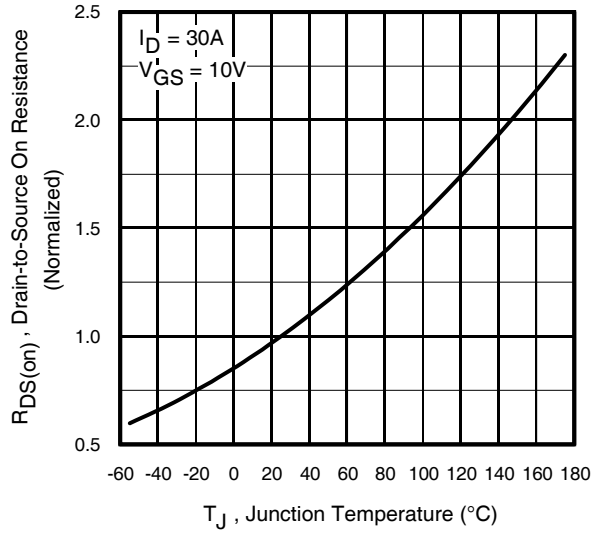

Fig 8. Maximum Safe Operating Area

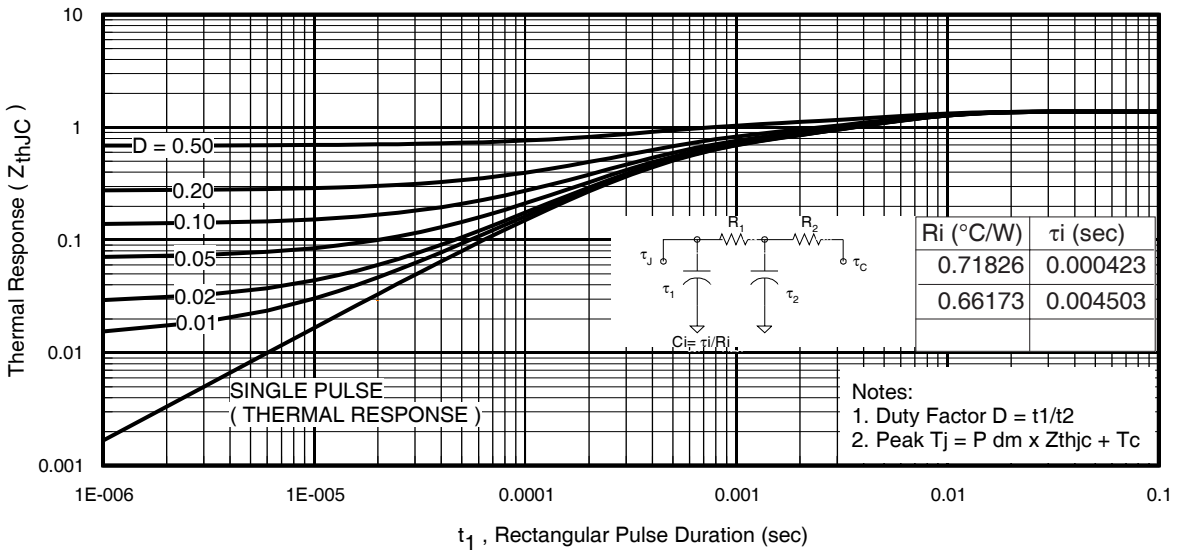4   www.kersemi.com

Fig 9. Maximum Drain Current Vs.
Case Temperature

Fig 10. Normalized On-Resistance
Vs. Temperature

Ri (°C/W)	τi (sec)
0.71826	0.000423
0.66173	0.004503

Notes:
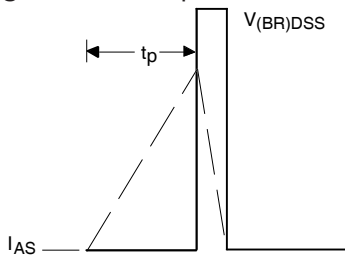1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
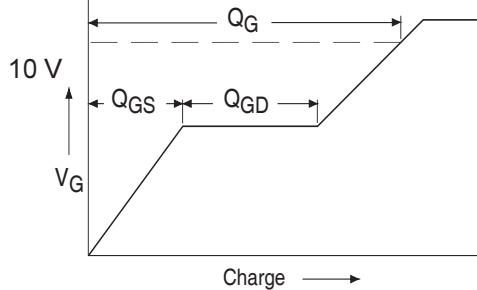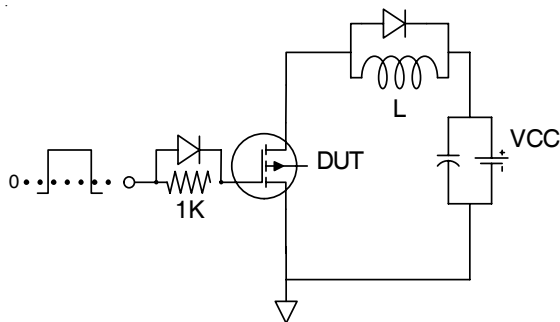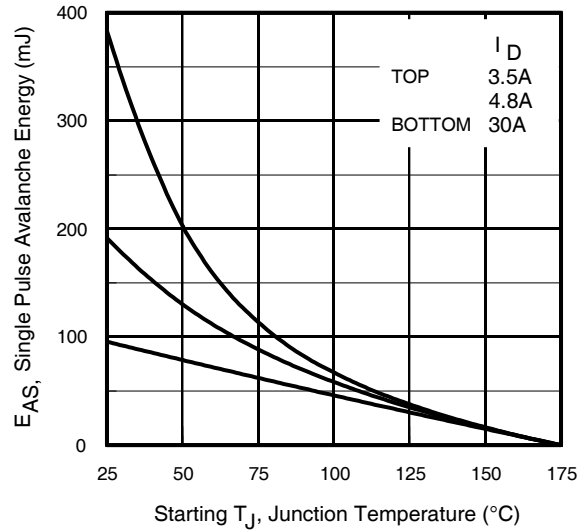
IRFR/U2607Z

Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

I_D
TOP 3.5A
4.8A
BOTTOM 30A

Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

I_D = 1.0A
I_D = 1.0mA
I_D = 250µA
ID = 50µA

Fig 14. Threshold Voltage Vs. Temperature

6

Fig 15. Typical Avalanche Current Vs.Pulsewidth

Duty Cycle = Single Pulse

0.01

0.05

0.10

Avalanche Current (A)

tav (sec)

Allowed avalanche Current vs avalanche pulsewidth, tav assuming ΔTj = 25°C due to avalanche losses. Note: In no case should Tj be allowed to exceed Tjmax

TOP   Single Pulse
BOTTOM   1% Duty Cycle
I_D = 30A

E_{AR} , Avalanche Energy (mJ)

Starting T_J , Junction Temperature (°C)

Fig 16. Maximum Avalanche Energy
Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
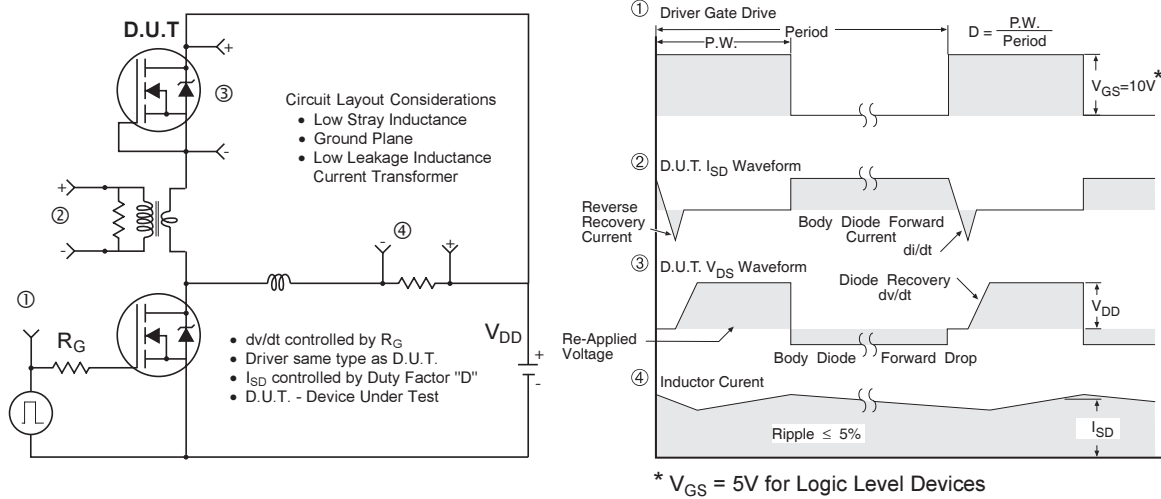**(For further info, see AN-1005 at www.irf.com)**
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
   $t_{av\ =}$ Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   Z_{thJC}(D, t_{av}) = Transient thermal resistance, see figure 11)

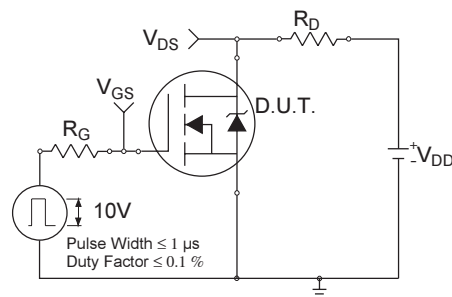$$P_{D\ (ave)} = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
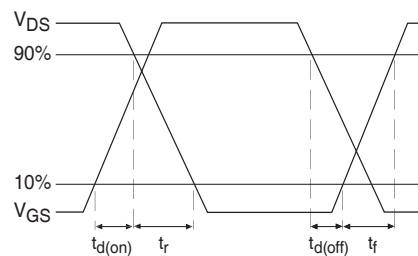$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 18a. Switching Time Test Circuit
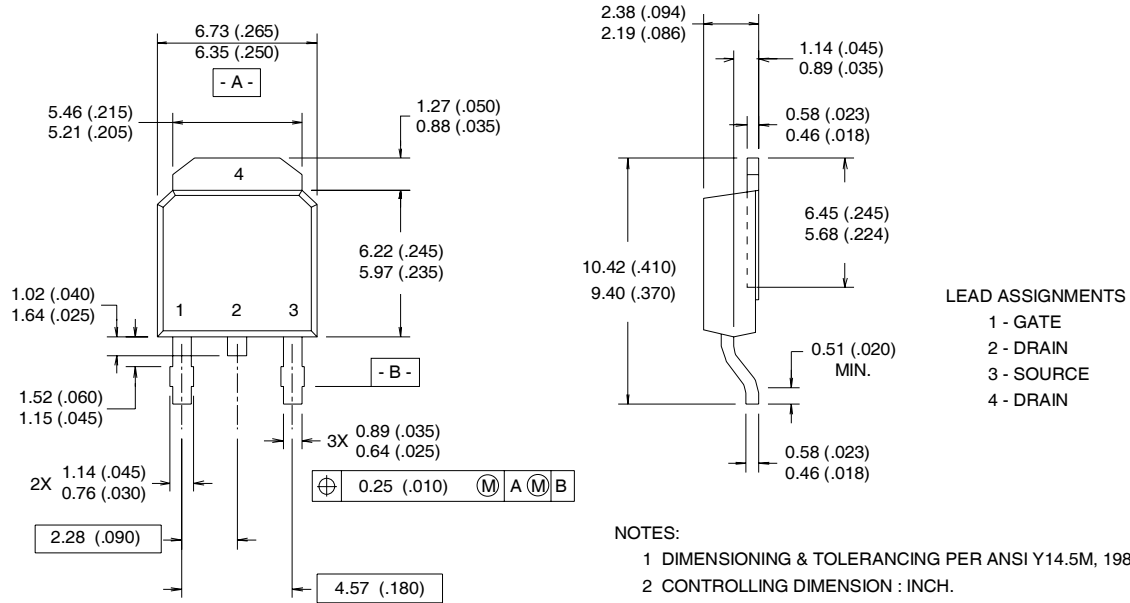

Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline
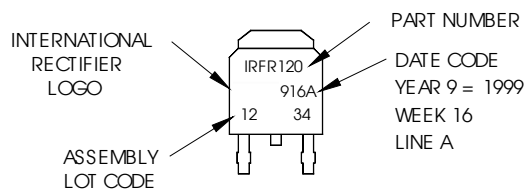
Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)

- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

6.22 (.245)
5.97 (.235)

1.02 (.040)
1.64 (.025)

1   2   3

- B -

1.52 (.060)
1.15 (.045)

3X 0.89 (.035)
0.64 (.025)

2X 1.14 (.045)
0.76 (.030)

⊕ | 0.25 (.010) | Ⓜ | A Ⓜ | B

2.28 (.090)

4.57 (.180)

2.38 (.094)
2.19 (.086)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

10.42 (.410)
9.40 (.370)

0.51 (.020)
MIN.

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
   SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 1234
          ASSEMBLED ON WW 16, 1999
          IN THE ASSEMBLY LINE "A"

          Note: "P" in assembly line
          position indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRFR120
916A

12   34

DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

ASSEMBLY
LOT CODE

OR

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

IRFR120
P916A

12   34

DATE CODE
P = DESIGNATES LEAD-FREE
    PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 16
A = ASSEMBLY SITE CODE

ASSEMBLY
LOT CODE

IRFR/U2607Z

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)
- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

6.22 (.245)
5.97 (.235)

1.52 (.060)
1.15 (.045)

1   2   3

- B -

2.28 (.090)
1.91 (.075)

9.65 (.380)
8.89 (.350)

3X 1.14 (.045)
0.76 (.030)

3X 0.89 (.035)
0.64 (.025)

| ⊕ | 0.25 (.010) | Ⓜ | A | Ⓜ | B |

2.28 (.090)
2X

2.38 (.094)
2.19 (.086)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
  1 - GATE
  2 - DRAIN
  3 - SOURCE
  4 - DRAIN

NOTES:
  1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  2 CONTROLLING DIMENSION : INCH.
  3 CONFORMS TO JEDEC OUTLINE TO-252AA.
  4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
     SOLDER DIP MAX. +0.16 (.006).
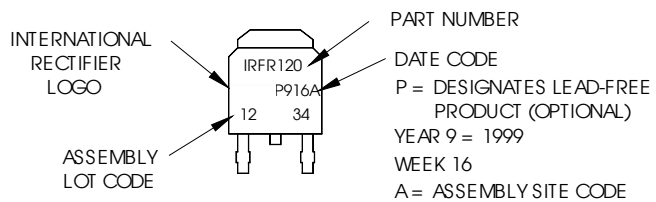
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
          WITH ASSEMBLY
          LOT CODE 5678
          ASSEMBLED ON WW 19, 1999
          IN THE ASSEMBLY LINE "A"
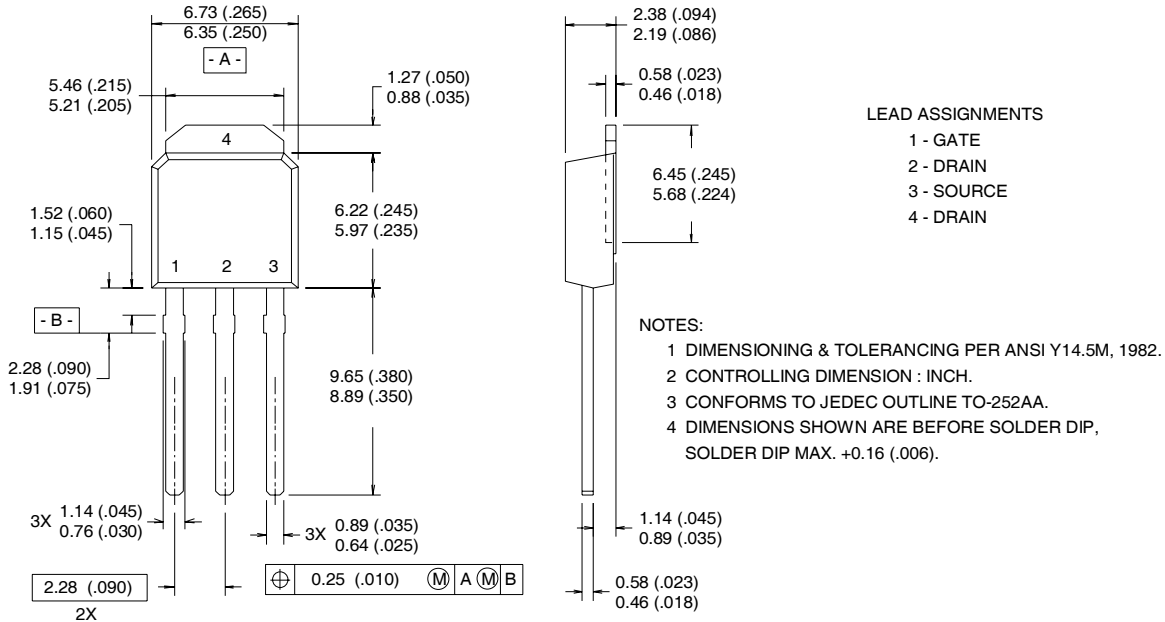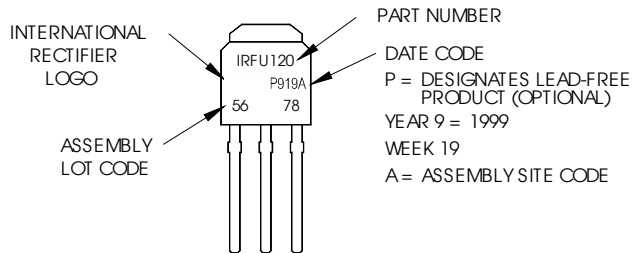
Note: "P" in assembly line
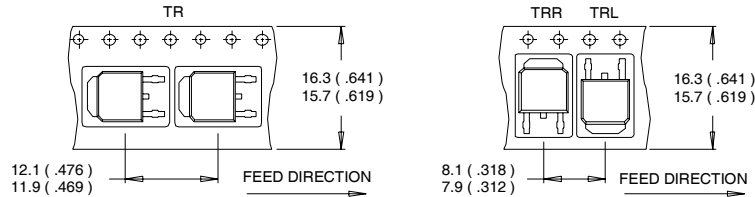position indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
919A
56   78

ASSEMBLY
LOT CODE

PART NUMBER

DATE CODE
YEAR 9 = 1999
WEEK 19
LINE A

OR

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
P919A
56   78

ASSEMBLY
LOT CODE

PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE
    PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 19
A = ASSEMBLY SITE CODE

www.kersemi.com

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TR

16.3 (.641)
15.7 (.619)

12.1 (.476)
11.9 (.469)

FEED DIRECTION

TRR   TRL

16.3 (.641)
15.7 (.619)

8.1 (.318)
7.9 (.312)

FEED DIRECTION

NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

$\varnothing$ 13 INCH

16 mm

NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by
max. junction temperature. (See fig. 11).

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.21mH
R_G = 25Ω, I_{AS} = 30A, V_{GS} =10V. Part not
recommended for use above this value.

③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time
as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive
avalanche performance.

⑥ This value determined from sample failure population. 100%
tested to this value in production.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to
application note #AN-994

⑧ R_θ is measured at T_J approximately 90°C